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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/342,235	06/29/1999	YASUHIKO TAKEMURA	0756-1980ELE	6257

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EXAMINER	
SEFER, AHMED N	
ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 09/09/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/342,235	TAKEMURA, YASUHIKO	
	Examiner	Art Unit	
	A. Sefer	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *6/23/04*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *6-11 and 13-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *6-11* is/are allowed.

6)☒ Claim(s) *13-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/15/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on June 23, 2004 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

3. Claims 13-19, 24 and 25 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki et al. ("Yamazaki") USPN 6,331,723.

Yamazki discloses (figs. 5-7, col. 5, lines 36-52 and claims 1) a semiconductor device comprising a substrate having an insulating surface; at least first and second semiconductor islands 502 and 503 comprising polysilicon (as in claims 14 and 17) formed directly on said insulating surface wherein each of the semiconductor islands has a channel region and a pair of impurity regions 517-520; a first and a second gate insulating film 512 formed over said semiconductor island, respectively; at least first and second gate electrodes 506/507 formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; a wiring for electrically connecting one of the impurity

regions of the first semiconductor island with the second gate electrode; an interlayer insulating film 521 formed over a wiring (as in claims 16 and 19); a pixel electrode (not shown) formed over said interlayer insulating film (as in claim 16) and electrically connected to one of the pair of the impurity regions of the second semiconductor island, wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of PTFT.

As for claims 15 and 18, Yamazaki discloses (fig. 7C) a data line electrically connected to the other one of the impurity regions of the first semiconductor island.

As for claim 19, Yamazaki discloses a gate electrode and impurity region formed below a interlayer insulating film making it inherent that said wiring connecting said gate electrode and one of said impurity regions has to be located below said interlayer insulating film.

As for claims 24 and 25, Yamazaki discloses (see claims 1, 23 and 34) a voltage supply line electrically connected to the other one of the pair of the impurity regions of the second semiconductor island.

4. Claims 20-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Yamazaki.

Yamazki discloses (figs. 5-7, col. 5, lines 36-52 and claims 1) a semiconductor device comprising a substrate having an insulating surface; at least first and second semiconductor islands 502 and 503 comprising polysilicon (as in claim 21) formed directly on said insulating surface wherein each of the semiconductor islands has a channel region and a pair of impurity regions 517-520; a first and a second gate insulating film 512 formed over said semiconductor island, respectively; at least first and second gate electrodes 506/507 formed over said first and second semiconductor islands respectively with said first and second gate insulating films interposed therebetween; a wiring for electrically connecting one of the impurity regions of the

first semiconductor island with the second gate electrode; a surface smoothing film 521 formed over said wiring; a pixel electrode (not shown) formed over said surface smoothing film (conventional) and electrically connected to one of the pair of the impurity regions of the second semiconductor island, wherein the first semiconductor island is a part of an NTFT and the second semiconductor island is a part of PTFT.

As for claim 22, Yamazaki discloses (fig. 7C) a data line electrically connected to the other one of the impurity regions of the first semiconductor island.

As for claim 23, Yamazaki discloses a gate electrode and impurity region formed below a surface smoothing film making it inherent that said wiring connecting said gate electrode and one of said impurity regions has to be located below said surface smoothing film.

Allowable Subject Matter

5. Claims 6-11 are allowed.

6. The following is a statement of reasons for the indication of allowable subject matter: The prior art fails to disclose the device structure as recited in claims 6, 9, 10 and 11. Specifically, the prior art neither teaches nor makes obvious the claimed device structure of claims 6, 9, 10 and 11.

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Namura et al. USPN 4,602,192 disclose a TFT including a plurality of transistors having a gate electrode of one transistor connected to an impurity region of another.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to A. Sefer whose telephone number is (571) 272-1921.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272-1915.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NATHAN J. FLYNN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800

ANS
August 31, 2004